REMARKS

Section 103 Rejections

Claims 1-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ziger U.S. Patent 6,498,640, and further in view of Stirton et al. U.S. Patent 6,614,540.

Claims 8-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ziger U.S. Patent 6,498,640, and further in view of Stirton et al. U.S. Patent 6,614,540.

Claims 1-16, 18, and 20-21 are now in the application. Claims 2-7, 9-10, and 15-16 have been amended. Claims 17 and 19 have been cancelled. New claims 20 and 21 have been added.

Claims 17 and 19 were objected to because of the following informalities: The claims include the step of forming a layer of metal interconnects over the first layer on the integrated circuit substrate. However, the term "metal interconnects" related to a "further layer of integrated circuit" was not found in the specification. Claims 17 and 19 have been amended.

THE REFERENCES

A. The Ziger Reference

Ziger U.S. Patent 6,498,640 describes a method for facilitating alignment measurements in a semiconductor fabrication process that uses a combination of underlying and latent images on a substrate to indicate alignment between a lithographic mask and the substrate. In an example embodiment of the method for measuring alignment, a substrate having a layer of photoresist disposed on it, is illuminated through a reticle element resulting in the formation of a first plurality of underlying grating images. The first plurality of images has a repetitive and

symmetrical pattern with equal spacing between images. A second plurality of latent grating images is formed in the photoresist having substantially the same pattern of images as the first plurality of images. The second plurality of images is disposed above from the first plurality of images, the first and second plurality of images serving as an indicator of alignment between the mask and the substrate when the combined images forming a repetitive pattern. The system includes an energy source, an optical element, and a reticle element for forming the plurality of images on the substrate to aid in alignment.

B. **The Stirton et al. Reference**

Stirton et al. U.S. Patent 6,614,540 teaches a method for characterizing features including measuring a dimensional characteristic of a first grating structure; illuminating at least a portion of a first feature and the first grating structure, the first feature being formed over at least a portion of the first grating structure; measuring light reflected from the illuminated portion of the first feature and the first grating structure to generate a reflection profile; selecting at least one reference reflection profile based on the measured dimensional characteristic of the first grating structure, comparing the generated reflection profile to the selected reference reflection profile; and determining a characteristic of the first feature based on the comparison between the measured reflection profile and the selected reference reflection profile.

The present invention provides a process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate comprises the steps of forming a test pattern in selected fields of a first layer on a semiconductor substrate, forming a layer of photoresist over the first layer, forming latent images in portions of the photoresist layer lying in the selected fields overlying the test pattern of the first layer; and measuring the alignment of the test pattern in the selected fields of the first layer with the overlying latent images in the photoresist layer using

scatterometry. In a preferred embodiment, the test pattern formed in each of the selected fields in the first layer comprises a pattern of parallel spaced apart lines, and the latent images formed in the portions of the photoresist layer in the selected fields above the test pattern in the first layer also comprises a pattern of parallel spaced part lines, with the two sets of lines interspaced between one another and generally parallel to one another to form a diffraction pattern.

The combination of using latent images (rather than developed images) formed in the photoresist layer; and by using only alignment marks in selected fields (rather than the entire substrate), the alignment can be carried out without expending the entire wafer or substrate as a test or alignment wafer. In other words, the remaining fields on the wafer or substrate not utilized in the alignment, can still be used to form chips, thus raising the overall yield of chips obtained from a given set of wafers including the test wafer.

DISCUSSION

Claims 1-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ziger U.S. Patent 6,498,640, and further in view of Stirton et al. U.S. Patent 6,614,540. Claims 8-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ziger U.S. Patent 6,498,640, and further in view of Stirton et al. U.S. Patent 6,614,540.

As stated above, and also on page 7, line 27 to page 8, line 28 of Applicants' specification, Applicants' claimed invention is characterized by the synergistic combination of the use of latent (undeveloped) images in a photoresist layer and alignment marks in an underlying substrate to check the alignment of the photoresist images with the substrate using only selected fields or stepper positions whereby the remainder of the fields on the wafer or substrate may be used for conventional processing after completion of the alignment.

If the latent images had been developed during the alignment process, or had the entire wafer been used in the alignment step, there would be no further utilization of the particular wafer, i.e., the wafer could only function as a test wafer, thus wasting the remainder of the wafer.

By only using selected fields of the semiconductor wafer distributed across the face of the wafer to form the test patterns of lines, as shown at arrows A-D in Figure 6, and then not developing the latent images formed in those fields in order to align the two layers to one another, and by exploiting the ability of scatterometry technology to detect latent images, only selected fields of a wafer need be used to align an underlying pattern of parallel spaced apart metal lines with a pattern of latent images of lines in an overlying photoresist layer.

Thus, with the alignment process of the invention, rather than expending an entire test wafer and then relying on the alignment adjustments made on such a wafer to suffice for the remaining wafers in the same batch, if desired each wafer may be subject to the alignment process of the invention to detect and then correct any misalignment detected in the test fields by the scatterometry apparatus, following which the other fields in the same wafer (which should now be precisely aligned) may be used to form the desired layer over the underlying integrated circuit structure.

It should also be noted that the process of the invention makes it possible to utilize two sets of test fields on a particular wafer, if desired. That is, a first set of test fields may be used, as described, to verify the alignment of the reticle with the underlying layer using the latent images formed by the reticle in the photoresist layer, followed by adjustment of the reticle. Then, a second set of latent images of lines could be formed in a second set of test fields in the same wafer to verify that the corrections already made are satisfactory. Since this would expend, for example, 8 fields instead of only 4, it may be more desirous to only use one set of test fields.

However, in view of the fact that wafers such as the 8" diameter wafers currently in production, have as many as 200 fields, the expenditure of an extra 4 fields may be deemed to be a small price to pay for verification of the accuracy of the alignment.

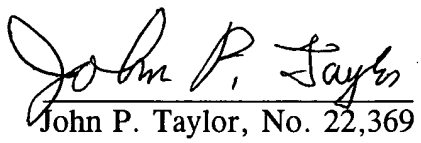
The alignment process of the invention utilizes only a small number of selected test fields on the wafer and the overlying photoresist layer for the alignment of the wafer to thereby preserve the remainder of the fields on the wafer and in the photoresist layer for conventional processing.

Furthermore, by using scatterometry technology to analyze the alignment of the pattern in the photoresist with the alignment marks in the underlying wafer, a pattern of ***latent images*** (such as parallel lines) may be formed in the overlying photoresist layer, and this pattern of ***latent images*** may then be aligned with an underlying pattern (such as parallel lines) formed in selected test fields on the underlying semiconductor wafer since scatterometry technology is sensitive latent images as well as developed images. The remaining fields on the same wafer may then be utilized to form the desired integrated circuit structures on the wafer tested.

Thus, the process of the invention, by combining the use of selected test fields in the wafer (rather than the entire wafer) with the formation of latent images in the overlying photoresist layer, and scatterometry technology to detect such latent images, avoids the need for expenditure of an entire test wafer to verify the alignment and also permits each individual wafer to be tested for alignment, and corrected where needed. Nothing in the cited references suggests this novel combination of steps to achieve the stated desired result.

Applicants respectfully submit that Claims 1-16, 18, and 20-21 are patentable over the prior art and the objections in the Office Action. If the Examiner in charge of this case feels that there are any remaining unresolved issues in this case, the Examiner is urged to call the undersigned attorney at the below listed telephone number which is in the Pacific Coast Time Zone.

Respectfully Submitted,



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